## 10/006398 10/006398

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PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

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	APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	-	EXAMINER				
ì	10006398	11/30/2001	356	401	2877	Laure	h voo a .				
	**APPLICANTS: Yates Colin; Pasch Nicholas; Eib Nicholas;										
	"CONTINUING DATA VERIFIED: Nove \$\frac{1}{25} \left  03										
	** FOREIGN AF	PLICATIONS VER	RIFIED:	uone	L	ge a	7/25/05				
PG-PUB DO NOT PUBLISH ☑ RESCIND □											
F	oreign priority claim	ed	□ yes	AND ASSESSMENT OF THE PERSON O		ATTORN	NEY DOCKET NO				
	5 USC 119 conditio	ns met ledged Examiners's intid	- yes	no			*				
F	ITLE : Alignmen	nt process for integ	rated circ	ui: structures :	3D 50=	01-234					
TITLE: Alignment process for integrated circuit structures on semiconductor substrate using scatterometry measurements of latent images in spaced apart test fields on substrate											
3.5.5. Or COMM.IPAL. (MIPO-435L (Rev. 12-94))											

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED						
	Assistant Examiner	Total Claims	Pri	nt Claim for				
ISSUE FEE		DRAWING						
Amount Due Date Paid		Sheets Drwg:		Print Fig.				
	Primary Examiner							
TERMINAL	PREPARED FOR ISSUE	Application Examiner						
DISCLAMER	WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.							

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